CLAIMS

1 A program tool for the generation of a large scale integrated circuit, said tool comprising the steps of

(a) defining an architecture comprising a multiplicity of data handling cores and at least one shared memory system.

(b) defining interconnect logic separately from said cores, said interconnect logic defining, in accordance with data transfer requirements of said cores, data paths that require data transfers between cores to proceed by way of a shared memory system

2 A program tool according to claim 1 wherein said interconnect logic prescribes a hierarchy of data aggregation whereby each core is coupled to a memory by way of at least one level of arbitration and at least some cores are coupled to said memory by way of at least two levels of arbitration

3 A program tool according to claim 1 and wherein the tool provides the step of defining register paths separate from data transfer paths and proceeding between data processor cores and others of said cores

4 A program tool according to claim 1 and wherein the tool provides the step of defining control paths separate from data transfer paths

5 A program tool according claim 1 wherein the tool further comprises the steps of

obtaining said cores from a library of cores, and

defining parameters for each of said cores

6 A program tool for the generation of a large scale integrated circuit, said tool comprising the steps of

(a) defining an architecture comprising a multiplicity of data handling cores and at least one shared memory system,

(b) obtaining said cores from a library of cores,

(c) defining interconnect parameters for each of said cores, and

(d) configuring automatically in accordance with said parameters interconnect logic separately from said cores, said interconnect logic defining data transfer paths that require data exchanges between cores to proceed by way of at least one shared memory system

7 A program tool according to claim 6 and wherein the tool provides the step of defining register paths separate from the data transfer paths and proceeding between data processor cores and others of said cores

8 A program tool according to claim 7 and wherein the tool provides the step of defining control paths separate from the data transfer paths

9 A program tool according to claim 6 wherein said interconnect logic prescribes a hierarchy of data aggregation whereby each core is coupled to said memory by way of at least one level of arbitration and at least some cores are coupled to said memory by way of at least two levels of arbitration

10 A program tool according to claim 6 and further comprising reprogramming said interconnect parameters to optimize a layout for said circuit